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DS50002627B

High-Performance WQVGA Display Module with maXTouch® Information Sheet

The High-Performance WQVGA Display Module with maXTouch (AC320005-4) is designed for evaluating the Microchip graphics display solution and graphics library for 32-bit microcontrollers. This board is compatible with Multimedia Expansion Board II (DM320005-2), as well as with Xplained Pro and Xplained Ultra. This board has a TFT 480 x 272 display with 24-bit parallel RGB interface with maXTouch capacitive touch interface.

Features

- 480 x 272 TFT display
- maXTouch MXT336
- QTouch® QT1070 (with four navigation keys)
- 4 K-bit 1-wire EEPROM
- Integrated Projective Capacitive Touch (PCAP) panel

Running the High-Performance WQVGA Display Module with maXTouch Demonstration Code

For free Microchip demonstration code and additional information, please visit the MPLAB® Harmony web page at: www.microchip.com/Harmony.

After MPLAB Harmony is installed, refer to the following MPLAB Harmony installation folder for the demonstration purpose:

`C:\microchip\harmony\<version_number>\apps\gfx`.

To work with older Xplained Pro and Xplained Ultra development boards, disconnect the ribbon connector from the adapter board and connect it to the GFX port (50 flex) of the Xplained Pro or Xplained Ultra.

FIGURE 1: WQVGA DISPLAY MODULE BLOCK DIAGRAM

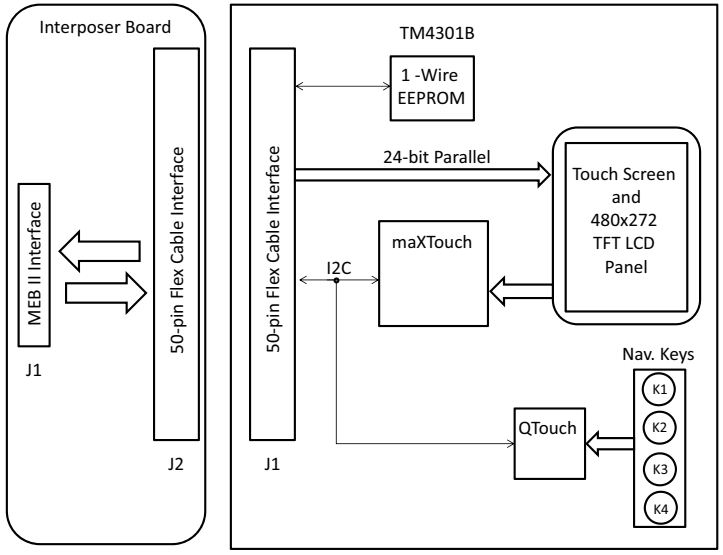
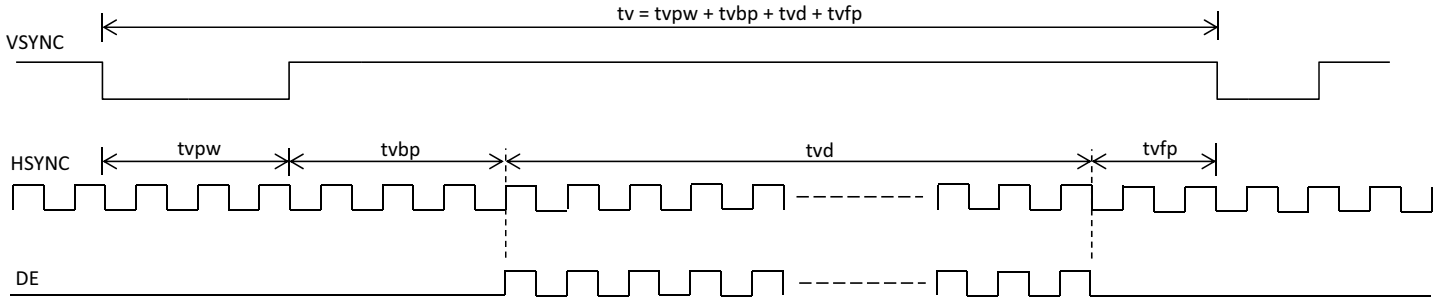
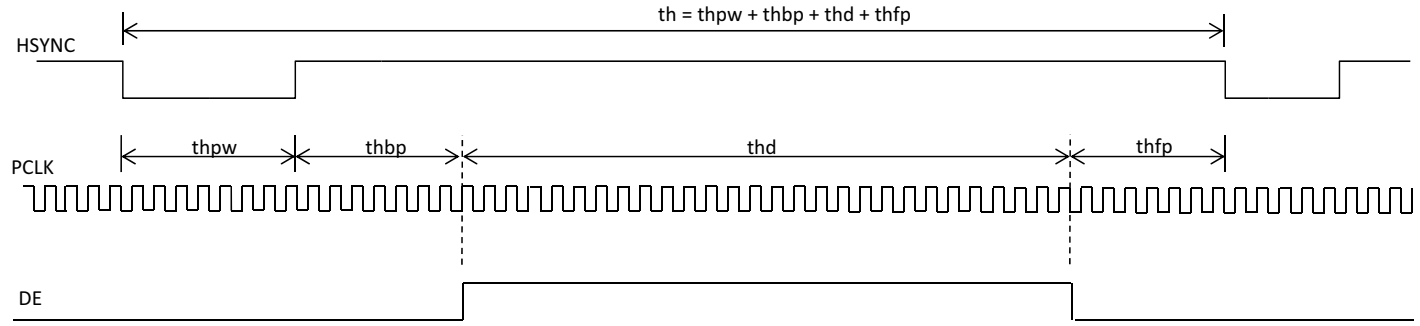


TABLE 1: TIMING SPECIFICATION VALUES

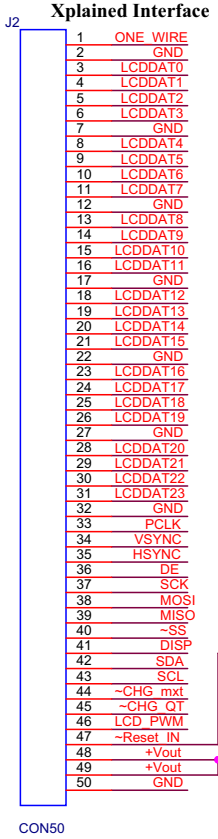
Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock Cycle	1/PCLK	-	9	15	MHz
Hsync Cycle	1/th	-	17.14	-	kHz
Vsync Cycle	1/tv	-	59.94	-	Hz
Horizontal Signals					
Horizontal Cycle	th	525	525	605	CLK
Horizontal Display Period	thd	480	480	480	CLK
Horizontal Front Porch	thfp	2	2	82	CLK
Horizontal Pulse width	thpw	2	41	41	CLK
Horizontal Back Porch	thbp	2	2	41	CLK
Vertical Signals					
Vertical Cycle	tv	285	286	399	Hsync
Vertical Display Period	tvd	272	272	272	Hsync
Vertical Front Porch	tvfp	1	2	227	Hsync
Vertical Pulse Width	tvpw	1	10	11	Hsync
Vertical Back Porch	tvbp	1	2	11	Hsync

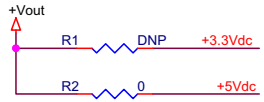




Bottom Contacts
Use Type 1 FFC

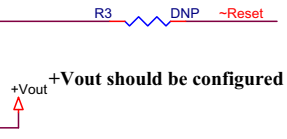
Xplained Interface





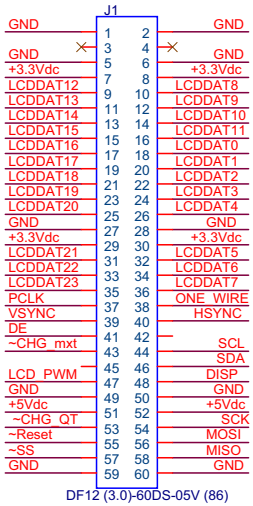
~CHG_QT is connected to Pin 53 for future use if desired.

SCK, MOSI, MISO and ~SS are connected to Pins 54, 56, 58 and 57 (respectively) for future use if desired.



+Vout should be configured for +5Vdc.

MEB II Interface



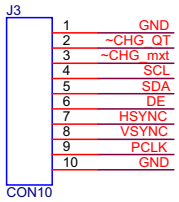
ONE_WIRE is connected to Pin 38 for future use if desired.

Microchip "LCD_CS" is not used by PDA LCD interface

Microchip "LCD_Reset" is connected to PDA "DISP". When DISP is low the LCD is in standby mode. When DISP is high the LCD is in normal display mode.

Should we connect Microchip "LCD_CS" to PDA "DISP"

Debug Header



Mounting Holes